REMARKS

Claims 1-9 are pending in this application. In the Office Action, the Examiner rejected claims 1-9 under 35 U.S.C. § 112, second paragraph. The Examiner also rejected claims 1, 4-5, 7, 8, and 9 under 35 U.S.C § 102(b). Applicant respectfully traverses these rejections. The Examiner also stated that Claims 2-3 and 6 would be allowable if rewritten to overcome the rejection under 35 U.S.C. § 112, second paragraph. For the reasons set forth below, Applicant believes that all the claims are in condition for allowance and notice to that effect is earnestly solicited.

Specification

The Specification has been amended at pages 3 and 4 to correct typographical errors. Applicants submit that no new matter has been added. Examiner approval is respectfully requested.

Claim Rejections under 35 U.S.C. § 112, second paragraph.

The Examiner rejected claims 1-9 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

"One bit cell," "two bit cells," "three bit cells," and "maximum duration value"

The Examiner stated "In claim 1, it is unclear where the 'three bit cells', 'one bit cell', 'two bit cells' and 'maximum duration value' come from . . . ." Applicant respectfully traverses this rejection.

Claim 1 as filed states:

> 1. Apparatus for determining nominal pulse duration values in a signal encoded with an AES3 data stream, comprising:
>
> a first circuit for measuring duration of each pulse of the signal and providing a sequence of duration values, and
>
> a second circuit for detecting a maximum duration value, corresponding to duration of three bit cells, and providing first and second duration values corresponding to one bit cell and two bit cells respectively.

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The Specification explains at page 1 that "[A] signal encoded with an AES3 data stream is composed of pulses, and each pulse is one, two, or three bit cells in duration." Applicant believes that claim 1 as originally filed when read in view of the specification particularly points out and distinctly claims the subject matter which applicant regards as the invention.

Nonetheless, Applicant has amended claim 1 and claim 7 to explicitly recite an "AES3 data stream of data pulses, at least some of which comprise one of one bit cells, two bit cells and three bit cells" and to clarify that the "maximum duration value" is detected "from the sequence of duration values." Claims 4 and 9 have also been amended to explicitly recite an "AES3 data stream of data pulses, at least some of which comprise one of a half pulse, a whole pulse, or a wide pulse."

"First circuit," "second circuit," and "third circuit"

The Examiner stated:

> [I]t is unclear . . . how the recitation of "first circuit" and "second circuit" are read on the preferred embodiment. Insofar as understood, no such circuits can be determined on the drawings. The description of the present invention is incomplete because the first and second circuit are not connected to anything. Thus, the claimed apparatus may not perform the recited function. The same is true for claims 4, 6-7, and 9, and for reciting "third circuit" in claim 3.

Applicant respectfully traverses this rejection.

Applicant respectfully submits that the figure shows a combination of circuits which provide an apparatus for determining nominal pulse duration values in an AES3 data stream and an apparatus for extracting sample data values from a signal encoded with an AES3 data stream, as recited in claims 1 and 4 respectively.

- Claim 1

With respect to claim 1, the apparatus may measure the duration of a pulse for example through a "first circuit" which at least includes an edge detector 10 and a counter 14. See Specification, page 2, line 35 to page 3, line 7 (" . . . . the edge detector 10 and the counter 144 measure the length of each pulse.")

The apparatus may detect a maximum duration value (i.e. wide pulse value) and provide first and second duration values for example through a "second circuit" which at least includes a down counter 22, a comparator 26, and a register 30 and a look-up table 34. See Specification, page 3, line 23 to page 4, line 17. The Specification describe that:

> If the second count value were larger than the count value currently provided by the down counter, the comparator would provide a high output and the second count value would be loaded into the register and the downcounter 22 . . . . [T]he value loaded into the register will be the count value corresponding to the duration of the wide pulse of the input data stream.
>
> The value loaded into the register 30 is supplied to the address input of a lookup table 34. . . .

Specification, page 3, line 26 to page 4, line 11.

The claimed apparatus performs the recited function of "determining nominal pulse duration values" by "detecting a maximum duration value" and "providing first and second duration values" as recited in claim 1.

- Claim 3

With respect to claim 3, the apparatus may receive maximum, first, and second values, compare a measured duration value to the received values, and provide a corresponding output through a "third circuit" which may for example at least include a discriminator 18. See Specification page 4, lines 18-23 (". . . .the discriminator 18, which compares each count value . . . with the three reference values and provides an output . . . .")

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- Claim 4-6

With respect to claims 4-6, the "first circuit" may for example at least include an edge detector 10 and a counter 14. See Specification, page 2, line 35 to page 3, line 7 (" . . . . the edge detector 10 and the counter 144 measure the length of each pulse.") The "second circuit" may for example include a discriminator 18 that receives at least nominal pulse value (one bit, two bit or three bit nominal value) and compares a measured duration value with at least one nominal pulse duration value. See Specification page 4, lines 18-23.

The claimed apparatus performs the recited function of "extracting data values from a signal encoded with an AES3 data stream" by "comparing the measured duration value with at least one nominal pulse duration value to determine the duration of the pulse" as recited in claim 4.

Claim 2 Has Proper Antecedent Basis for "first and second duration values"

The Examiner stated that "In claim 2, the recitation 'the first and second duration values' lacks antecedent basis."

Applicants respectfully traverse this rejection. Claim 1 recites "first and second duration values" and thus provides proper antecedent basis for "the first and second duration values" recited in claim 2.

Accordingly, it is believed that the claims fully comply with § 112, second paragraph, and withdrawal of this rejection is respectfully requested.

Claim Rejections under 35 U.S.C § 102

The Examiner rejected claims 1, 4-5, 7, 8, and 9 under 35 U.S.C § 102 as being unpatentable over U.S. Patent No. 4,617,526 to Hikawa et al. The Examiner referred to the rejection as a 102(e) rejection. Applicants believe, however, that the rejection is actually a 102(b) rejection.

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The Examiner stated that "Figure 1B of Hikawa et al discloses a circuit having a first circuit (46, 47) and a second circuit (48, 50)." Applicant respectfully traverses this rejection.

Hikawa

Hikawa discloses a clock generator adapted to receive a digital bit stream having data bits and a synchronization code between prescribed numbers of data bits. A phase comparator determines the difference in phase between a clock pulse from a variable oscillator and a window pulse generated from the synchronization code. The phase comparator generates a phase control signal that represents the phase deviation of the clock from a window pulse A frequency comparator detects a synchronization code in the input bit stream to derive the frequency control signal by counting the number of clock pulses present in the period of the detected synchronization code. The phase control signal and frequency control signal are provided as inputs to the variable oscillator. See Hikawa at claim 1, at the specification, col. 2, lines 53-70 and col. 3, lines 1-19 and 31-39, and the abstract.

Claim 1

Hikawa does not teach or suggest each element required by the claims. For example, Hikawa et al. at least does not teach or suggest "a second circuit for detecting a maximum duration value, corresponding to duration of three bit cells, and providing first and second duration values corresponding to one bit cell and two bit cells respectively," as required by claim 1. Hikawa teaches a clock generator that synchronizes a clock with synchronization code in a bit stream but does not for example detect a maximum duration value as required by claim 1.

Claim 4

Claim 4 as amended recites "a second circuit for receiving at least one nominal pulse duration value, corresponding to nominal duration of one of a half pulse, whole pulse, or a wide pulse, and comparing the duration value of a pulse measured by the first circuit with at least one nominal pulse duration value . . ."

Hikawa at least does not teach or suggest "a second circuit" for "comparing the duration value of a pulse measured by the first circuit" of a pulse "with at least one nominal pulse duration value" that corresponds to a "nominal duration of a half pulse, whole pulse, or a wide pulse" as

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recited by claim 4. Hikawa compares a pulse duration to a synchronization code (11 bits) but does not compare a pulse duration value to a half pulse, whole pulse, or wide pulse value as required by claim 4.

Claim 7

With respect to claim 7, Hikawa at least does not teach or suggest "detecting a maximum duration value, corresponding to duration of three bit cells, and providing first and second duration values corresponding to one bit cell and two bit cells respectively," as required by claim 7. Hikawa teaches detecting a synchronization code in a bit stream for synchronizing a clock but does not teach detecting a maximum three-bit duration value and providing first (one bit) and second (two bit) duration values as required by claim 7.

Claim 9

Claim 9 as amended recites "a second circuit for receiving at least one nominal pulse duration value, corresponding to nominal duration of one of a half pulse, whole pulse, or a wide pulse."

Hikawa at least does not teach or suggest "comparing the measured duration value" of a pulse "with at least one nominal pulse duration value" that corresponds to a "nominal duration of a half pulse, whole pulse, or a wide pulse" as recited by claim 4. Hikawa teaches comparing a pulse duration to a synchronization code (11 bits) for synchronizing a clock but does not teach comparing a pulse duration value to a half pulse, whole pulse to determine the duration of the pulse relative to the nominal pulse duration value, or a wide pulse value as required by claim 9.

Dependent claims 2, 3, 5, and 8 are allowable at least because they depend from allowable independent claims.

Accordingly, it is believed that the claims fully comply with § 102(b), and withdrawal of this rejection is respectfully requested.

Summary

In summary, each of claims 1-9 are in condition for allowance and a notice of allowance is respectfully requested.

Respectfully submitted,

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